ISL9222AEVAL1Z Evaluation Board Application Manual

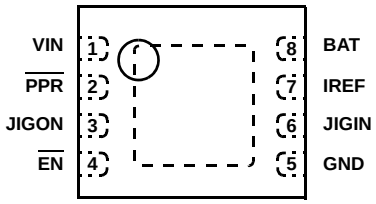
Application Note | December 4, 2008 | AN1445.0

Introduction

The ISL9222AEVAL1Z is an evaluation tool for the ISL9222A single-cell Li-ion battery charger. The evaluation tool provides a complete evaluation platform addressing all data sheet specifications and functionality. The jumpers on the board facilitate the programming of the charge current, different charging conditions, and can be used to make other necessary connections, such as current measurement.

The ISL9222A adds an additional feature in providing a limited amount of current to system architecture while protecting the system from destructively high voltage.

ISL9222A
(8 LD TDFN)
TOP VIEW



Ordering Information

PART NUMBER	DESCRIPTION
ISL9222AEVAL1Z	Evaluation Board for ISL9222A

Features

- A Complete Evaluation Platform for the ISL9222A Charger
- Both Inputs Accept Voltage up to 28V
- Flexible Power Connectors Each with a Hook and a Solder Pad Providing Variety to Users
- USB Port On-Board Accepts Power Directly From USB Cable
- Convenient Jumpers for Programming the Charge Current, Charge Mode, and for Current Measurement
- 3.5x2.5 Square Inches Board Size Handy for Evaluation
- Thermal Vias in the Thermal Pad Similar To Customers' Thermally Enhanced Environment
- On-Board LEDs for Input $\overline{PPR}$ and $\overline{CHG}$ State Indication
- RoHS compliant

What is Needed

The following instruments will be needed to perform testing:

- Power supplies:
  - PS1: DC 30V/2A
  - PS2: DC 10V/2A
  - PS3: DC 10V/2A
- DC Electronic load: 20V/2A
- Multimeters
- Oscilloscope
- Cables and wires

Quick Setup Guide (Refer to Figure 1)

Note: Do Not Apply Power Until Step 6

1. Connect a 5V supply PS1 to VDC input (J1, upper +) with the current limit set at 1.3A
2. Connect a 3.5V supply PS2 to BAT output (J2, upper +) with the current limit set at 1.3A
3. Connect a current meter to JP6 as shown in Figure 1
4. Connect the DC electronic load of 1.2A to VBAT (J2, upper +)
5. Insert a jumper shunt on JP3; all other jumper shunts are not installed
6. Turn on Power Supplies and DC electronic load, adjust the power supply PS2 such that the voltmeter V2 reads 3.5V
7. Voltmeter V3 at JIGON pin reads the voltage almost the same as voltmeter V2 reads. JIGON is the output of OR gate with VBAT as supply. JIGON will be pulled up to VBAT if the POR of the part is reached. Refer to the JIGON states table in the data sheet.
8. The LED should be on, indicating power on.
9. The current meter I2 should read about 0.25A as the charging current
10. Insert a jumper shunt on JP5 and the current meter I2 should read about 0.5A charging current
11. Insert a jumper shunt on both JP5 and JP7. The current meter I2 should read about 0.65A charging current
12. Reduce the voltage at PS2 to 2.0V for trickle charge currents. Repeat steps 8, 9 and 10. The current reading should be 50mA, 100mA and 190mA for steps 8, 9 and 10, respectively

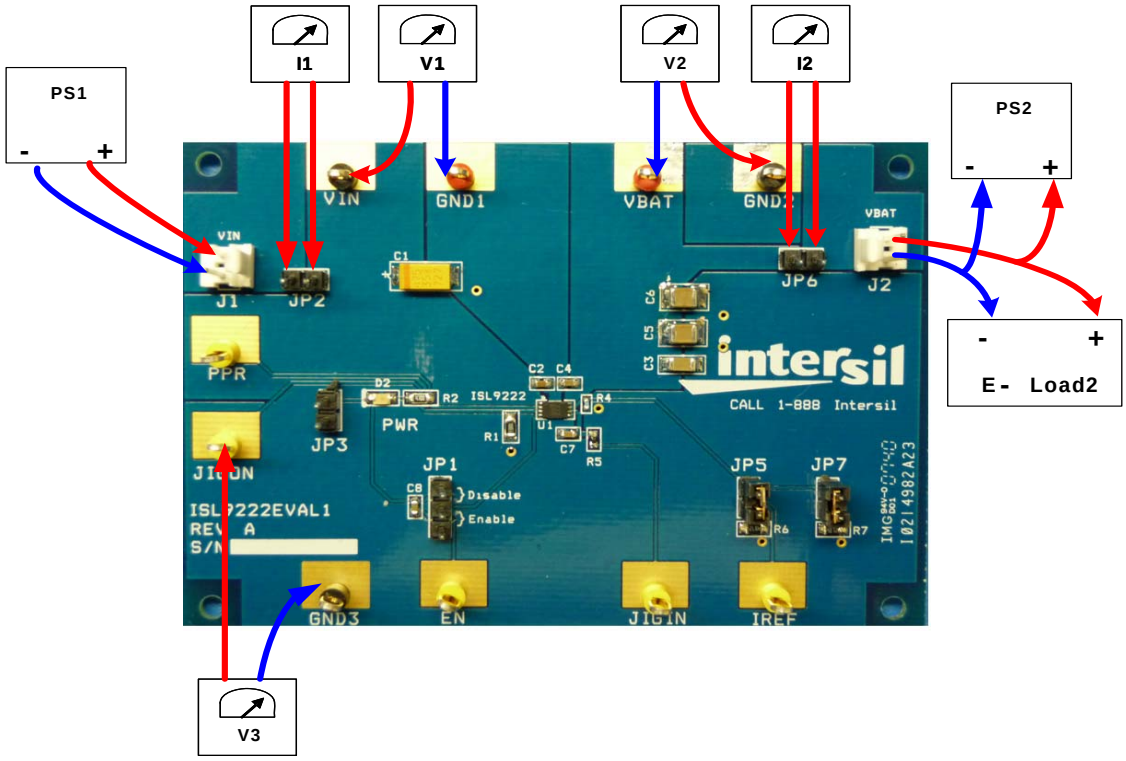


FIGURE 1. CONNECTION OF EQUIPMENT

Description of Jumper Settings

JP1 - Connects the $\overline{EN}$ pin to a pull-up voltage or GND. The pull-up voltage is either from the BAT voltage (when a shunt is installed on JP3) or from an external power supply. If there is no shunt installed on JP1, the $\overline{EN}$ pin is internally pulled down to logic LOW to enable the charger. If a shunt is installed across the two jumper pins labeled as “Enable”, the $\overline{EN}$ pin is driven to logic LOW, the charger is enabled, same as floating. If the shunt is installed across the two jumper pins labeled as “Disable”, the $\overline{EN}$ pin is driven to logic HIGH to disable the charger.

JP2 - A shunt installed on JP1 connects the input source from connector J1 to the circuit if input current measurement is not needed. The shunt can be replaced by a current meter if input current measurement is needed, as shown in Figure 1.

JP3 - Selects the power source for EN pin pull-up and LED supply. If a shunt is installed, the BAT voltage is selected to be the source, if not, an external power supply of 3.3V can be connected to upper pin to provide pull-up and LED supply voltage.

JP5 - Parallels an additional 48.7k resistor to the IREF pin such that the cradle charge current will be increased by 0.25A (R_{IREF} = 48.7k and the charge current is 0.25A if the shunts on both JP5 and JP7 are removed)

JP6 - A shunt installed on JP6 connects the BAT pin to the output connector J2 if output current measurement is not needed. The shunt can be replaced by a current meter if output current measurement is needed.

JP7 - Parallels an additional 48.7k resistor to the IREF pin such that the cradle charge current will be increased by 0.25A.

TABLE 1. JUMPER SETTING SUMMARY

JUMPER	POSITION	FUNCTION
JP1	Shunt installed	3-pin jumper. Installing shunt on the upper 2 pins connects EN pin to HI. Installing shunt on the lower 2 pins connecting EN pin to LOW.
JP2	Shunt installed	Connects input source from VIN connector to VIN pin.
JP3	Shunt installed	Connects cathode of D2 to VBAT for POR indication.
JP5	Shunt installed	Sets charge current to 0.5A if JP7 is not installed.
JP6	Shunt installed	Connects J2 to VBAT pin.
JP7	Shunt installed	Sets charge current to 0.5A if JP5 is not installed.

Board Design

Schematic

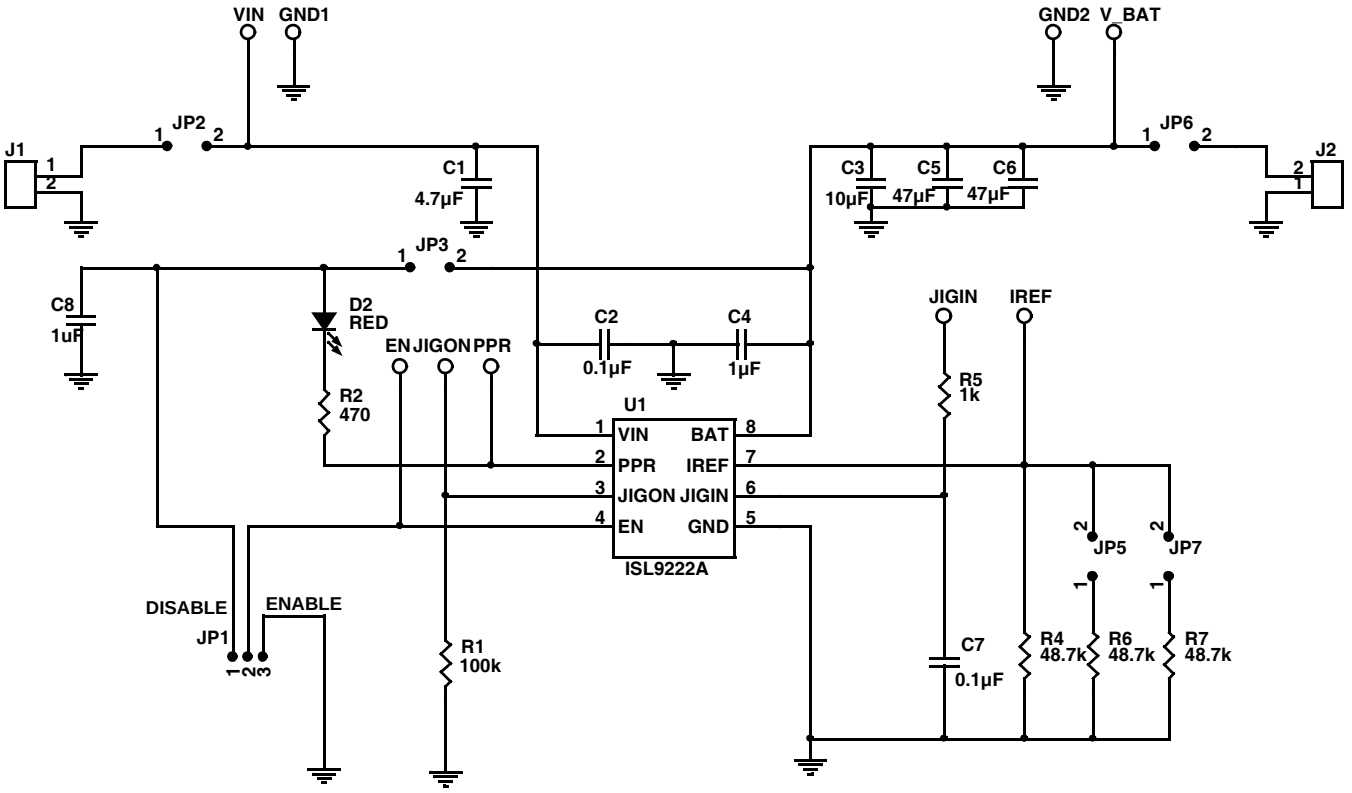


FIGURE 2. SCHEMATIC

TABLE 2. ISL9222AEVAL1Z BILL OF MATERIALS

ITEM	QTY	REFERENCE	PART DESCRIPTION	PART NO.	VENDOR
1	1	C1	4.7µF, 35V		Panasonic
2	3	C2, C4, C7	0.1µF, 50V		Panasonic
3	1	C3	10µF, 6.3µF		Panasonic
4	1	C8	1µF, 10V		Panasonic
5	2	C5, C6	47µF, 6.3V		Panasonic
6	1	D2	RED	SML-LXT0805GW-TR	Lumex
7	2	VIN, VBAT	Test Point, Red	5010	Keystone
8	5	PPR, JIGON, JIG IN, IREF, EN	Test Point, Yellow	5014	Keystone
9	1	GND	Test Point, Black	5011	Keystone
10	1	JP1	2.54mm Header, 3CKT	22-88-4030	Molex
11	5	JP2, JP3, JP5, JP6, JP7	2.54mm Header, 2CKT	22-28-4020	Molex
12	2	J1, J2	2.54mm Header, 2CKT	22-11-2022	Molex
13	1	R1	100k		Panasonic
14	1	R2	470		Panasonic
15	3	R4, R6, R7	48.7k		Panasonic
16	1	R5	1k		Panasonic
17	1	U1	ISL9222A	DFN 8L 2x3	Intersil

PCB Layout

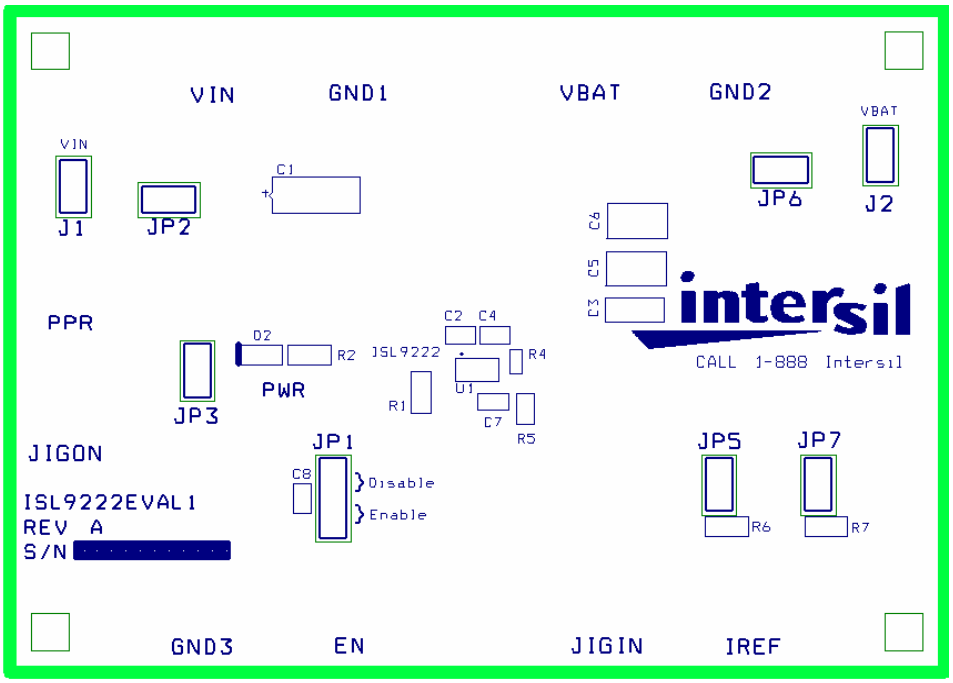


FIGURE 3. SILK LAYER

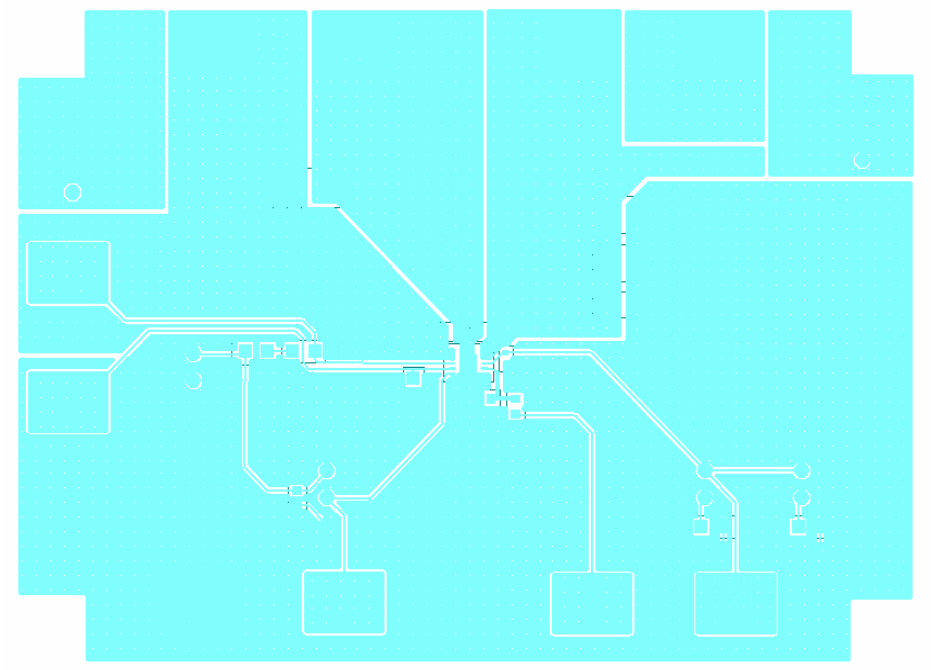


FIGURE 4. TOP LAYER

PCB Layout (Continued)

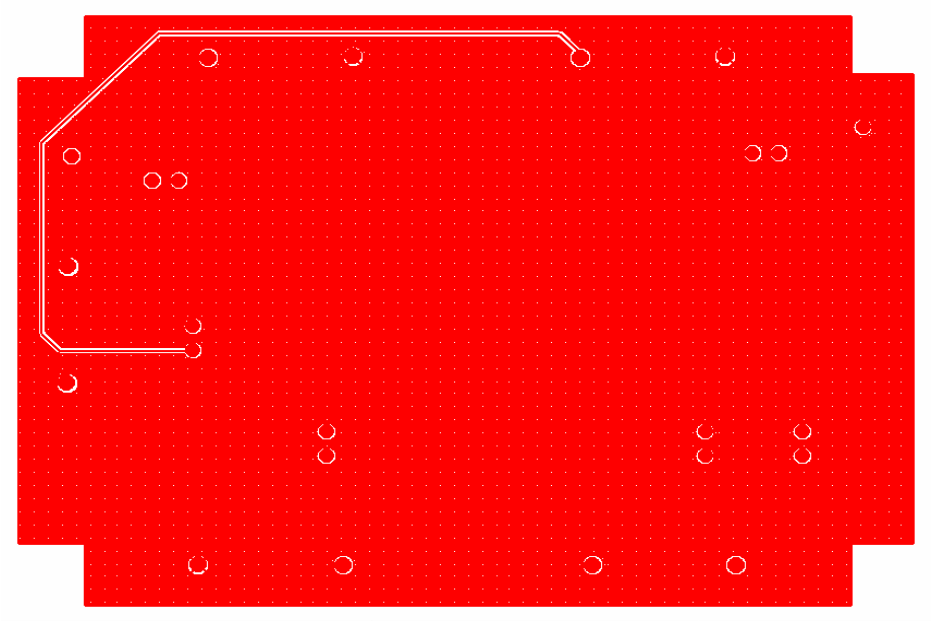


FIGURE 5. BOTTOM LAYER